DATA SHEET

TDA4866
Full bridge current driven vertical deflection booster

Preliminary specification
Supersedes data of August 1993
File under Integrated Circuits, IC02

1995 Aug 31

Philips Semiconductors

PHILIPS

Full bridge current driven vertical deflection booster

TDA4866

FEATURES

- Fully integrated, few external components
- No additional components in combination with the deflection controller TDA4850/51/55
- Pre-amplifier with differential high CMRR current mode inputs
- Low offsets
- High linear sawtooth signal amplification
- High efficient DC-coupled vertical output bridge circuit
- Powerless vertical shift
- High deflection frequency up to 140 Hz
- Power supply and flyback supply voltage independent adjustable to optimize power consumption and flyback time
- Excellent transition behaviour during flyback
- Guard circuit for screen protection.

GENERAL DESCRIPTION

The TDA4866 is a power amplifier for use in 90 degree colour vertical deflection systems for frame frequencies of 50 to 140 Hz. The circuit provides a high CMRR current driven differential input. Due to the bridge configuration of the two output stages DC-coupling of the deflection coil is achieved. In conjunction with TDA4850/51/55 the ICs offer an extremely advanced system solution.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply; note 1						
V_P	supply voltage (pin 3)		8.2	–	25	V
V_{FB}	flyback supply voltage (pin 7)	note 2	–	–	60	V
I_q	quiescent current (pin 7)		–	7	10	mA
Vertical circuit						
I_{defl}	deflection current (peak-to-peak value; pins 4 and 6)		0.6	–	2	A
I_{id}	differential input current (peak-to-peak value)	note 3	–	±500	±600	μA
Flyback generator						
I_{FB}	maximum current during flyback (peak-to-peak value; pin 7)		–	–	2	A
Guard circuit; note 1						
V_8	guard voltage	guard on	7.5	8.5	10	V
I_8	guard current	guard on	5	–	–	mA

Notes

1. Voltages refer to pin 5 (GND).
2. Up to 60 V ≥ V_{FB} ≥ 40 V a decoupling capacitor C_{FB} = 22 μF (between pin 7 and pin 5) and a resistor R_{FB} = 100 Ω (between pin 7 and V_{FB}) are required (see Fig.4).
3. Differential input current $I_{id} = I_1 - I_2$.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4866	SIL9P	plastic single in-line power package; 9 leads	SOT131-2

BLOCK DIAGRAM

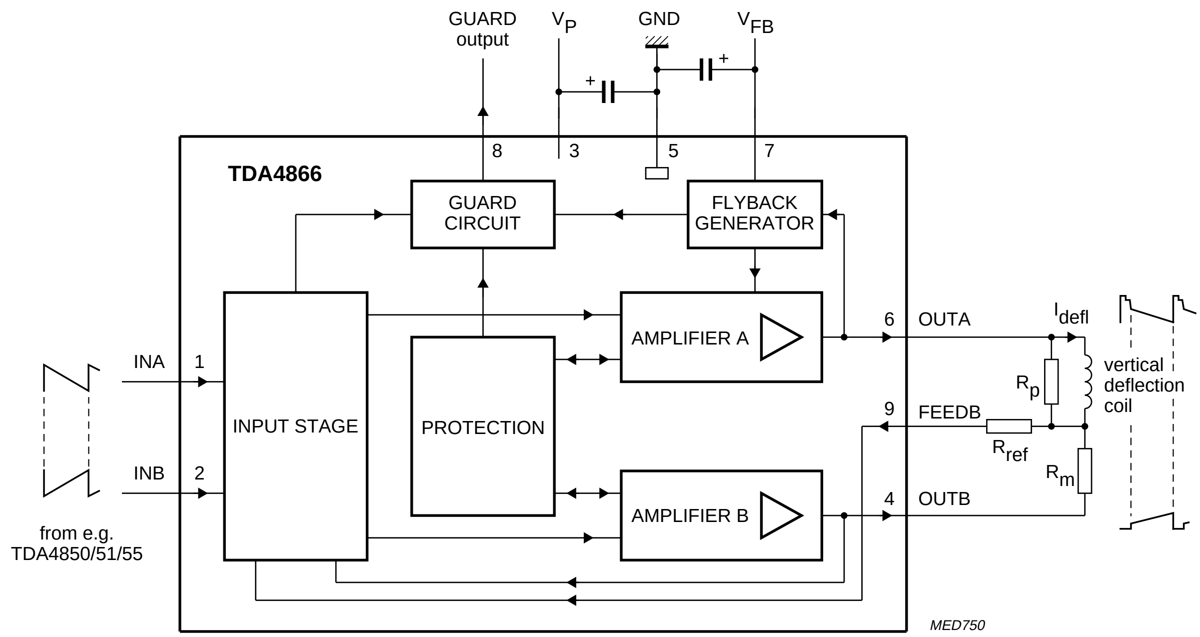


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INA	1	input A
INB	2	input B
V_P	3	supply voltage
OUTB	4	output B
GND	5	ground; note 1
OUTA	6	output A
V_{FB}	7	flyback supply voltage
GUARD	8	guard output
FEEDB	9	feedback input

Note

1. The mounting base is connected to pin 5 (GND).

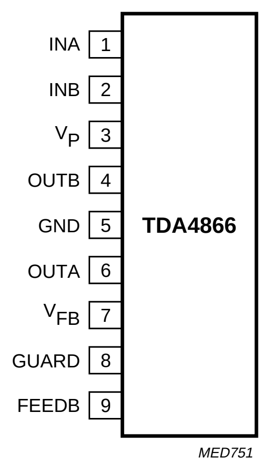


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4866 consists of a differential input stage, two output stages, a flyback generator, a protection circuit for the output stages and a guard circuit.

Differential input stage

The differential input stage has a high CMRR differential current mode input (pins 1 and 2) that results in a high electro-magnetic immunity and is especially suitable for driver units with differential (e.g. TDA4850/51/55) and single ended current signals. Driver units with voltage outputs are simply applicable as well (e.g. two additional resistors are required).

The differential input stage delivers the driver signals for the output stages.

Output stages

The two output stages are current driven in opposite phase and operate in combination with the deflection coil in a full bridge configuration. Therefore the TDA4866 requires no external coupling capacitor (e.g. 2200 µF) and operates with one supply voltage V_P and a separate adjustable flyback supply voltage V_{FB} only. The deflection current through the coil (I_{defl}) is measured with the resistor R_m which produces a voltage drop (U_{rm}) of: $U_{rm} \approx R_m \times I_{defl}$. At the feedback input (pin 9) a part of I_{defl} is fed back to the input stage. The feedback input has a current input characteristic which holds the differential voltage between pin 9 and the output pin 4 on zero. Therefore the feedback current (I_9) through R_{ref} is:

$$I_9 \approx \frac{R_m}{R_{ref}} \times I_{defl}$$

The input stage directly compares the driver currents into pins 1 and 2 with the feedback current I_9. Any difference of this comparison leads to a more or less driver current for the output stages. The relation between the deflection current and the differential input current (I_{id}) is:

$$I_{id} = I_9 \approx \frac{R_m}{R_{ref}} \times I_{defl}$$

Due to the feedback loop gain ($V_{U\,loop}$) and internal bondwire resistance (R_{bo}) correction factors are required to determine the accurate value of I_{defl}:

$$I_{defl} = I_{id} \times \frac{R_{ref}}{R_m + R_{bo}} \times \left(1 - \frac{1}{V_{U\,loop}}\right)$$

with $R_{bo} \approx 70$ mΩ and

$$\left(1 - \frac{1}{V_{U\,loop}}\right) \approx 0.98$$

for $I_{defl} = 0.7$ A.

The deflection current can be adjusted up to ±1 A by varying R_{ref} when R_m is fixed to 1 Ω.

High bandwidth and excellent transition behaviour is achieved due to the transimpedance principle this circuit works with.

Flyback generator

During flyback the flyback generator supplies the output stage A with the flyback voltage. This makes it possible to optimize power consumption (supply voltage V_P) and flyback time (flyback voltage V_{FB}). Due to the absence of a decoupling capacitor the flyback voltage is fully available.

Protection

The output stages are protected against:

- thermal overshoot
- short-circuit of the coil (pins 4 and 6).

Guard circuit

The internal guard circuit provides a blanking signal for the CRT. The guard signal is active HIGH:

- at thermal overshoot
- when feedback loop is out of range
- during flyback.

The internal guard circuit will not be activated, if the input signals on pins 1 and 2 delivered from the driver circuit are out of range or at short-circuit of the coil (pins 4 and 6).

For this reason an external guard circuit can be applied to detect failures of the deflection (see Fig.6). This circuit will be activated when flyback pulses are missing, which is the indication of any abnormal operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages referenced to pin 5 (GND) unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 3)	0	30	V
V_{FB}	flyback supply voltage (pin 7)	0	60	V
I_{FB}	flyback supply current	0	±1.8	A
V_1, V_2	input voltage	0	V_P	V
I_1, I_2	input current	0	±5	mA
V_4, V_6	output voltage	0	V_P	V
I_4, I_6	output current (note 1)	0	±1.8	A
V_9	feedback voltage	0	V_P	V
I_9	feedback current	0	±5	mA
V_8	guard voltage (note 2)	0	$V_P + 0.4$	V
I_8	guard current	0	±5	mA
T_{stg}	storage temperature	–20	+150	°C
T_{amb}	operating ambient temperature	–20	+75	°C
T_j	junction temperature (note 3)	–20	+150	°C
V_{es}	electrostatic handling for all pins (note 4)	–500	+500	V

Notes

1. Maximum output currents I_4 and I_6 are limited by current protection.
2. For V_P > 13 V the guard voltage V_8 is limited to 13 V.
3. Internally limited by thermal protection; switching point ≥ 150 °C.
4. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	4	K/W

CHARACTERISTICS

V_P = 15 V; T_{amb} = 25 °C; V_{FB} = 40 V; voltages referenced to pin 5 (GND); parameters are measured in test circuit (see Fig.3) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 3)		8.2	–	25	V
V_{FB}	flyback supply voltage (pin 7)	note 1	V_P + 6	–	60	V
I_{FB}	quiescent feedback current (pin 7)	no load; no signal	–	7	10	mA
Input stage						
$I_{id(p-p)}$	differential input current ($I_{id} = I_1 - I_2$) (peak-to-peak value)		–	±500	±600	μA
$I_{1, 2(p-p)}$	single ended input current (peak-to-peak value)	note 2	0	±300	±600	μA
CMRR	common mode rejection ratio	note 3	–	–54	–	dB
V_1	input clamp voltage	I_1 = 300 μA	2.7	3.0	3.3	V
V_2	input clamp voltage	I_2 = 300 μA	2.7	3.0	3.3	V
$TC_{i,1}$	input clamp signal TC on pin 1		0	–	±800	μV/K
$TC_{i,2}$	input clamp signal TC on pin 2		0	–	±800	μV/K
$V_1 - V_2$	differential input voltage	I_{id} = 0	0	–	±10	mV
I_9	feedback current		–	±500	±600	μA
V_9	feedback voltage		1	–	V_P – 1	V
$I_{id(offset)}$	differential input offset current ($I_{id(offset)} = I_1 - I_2$)	I_{defl} = 0; R_{ref} = 1.5 kΩ; R_m = 1 Ω	0	–	±30	μA
TC_{offset}	TC differential input offset shift		0	–	±50	nA/K
$C_{i\ INA}$	input capacity pin 1 referenced to GND		–	–	5	pF
$C_{i\ INB}$	input capacity pin 2 referenced to GND		–	–	5	pF
Output stages A and B						
I_4	output current		–	–	±1	A
I_6	output current		–	–	±1	A
V_6	output A saturation voltage to GND	I_6 = 0.7 A	–	1.3	1.5	V
		I_6 = 1.0 A	–	1.6	1.8	V
$V_{6,3}$	output A saturation voltage to V_P	I_6 = 0.7 A	–	2.3	2.9	V
		I_6 = 1.0 A	–	2.7	3.3	V
V_4	output B saturation voltage to GND	I_4 = 0.7 A	–	1.3	1.5	V
		I_4 = 1.0 A	–	1.6	1.8	V
$V_{4,3}$	output B saturation voltage to V_P	I_4 = 0.7 A	–	1.0	1.6	V
		I_4 = 1.0 A	–	1.3	1.9	V
LE	linearity error	I_{defl} = ±0.7 A; note 4	–	–	2	%
V_4	DC output voltage	I_{id} = 0 A; closed loop	6.6	7.2	7.8	V
V_6	DC output voltage	I_{id} = 0 A; closed loop	6.6	7.2	7.8	V
G_{oi}	open loop current gain ($I_{4,\ 6}/I_{id}$)	$I_{4,\ 6}$ < 100 mA; note 5	–	100	–	dB
G_{ofb}	open loop current gain ($I_{4,\ 6}/I_9$)	$I_{4,\ 6}$ < 100 mA; note 5	–	100	–	dB
G_{ifb}	current ratio (I_{id}/I_9)	closed loop	–	–0.2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{defl(ripple)}$	output ripple current as a function of supply ripple	$V_{P(ripple)}$ = ±0.5 V; I_{id} = 0; closed loop	–	±1	–	mA
Flyback generator						
$V_{7, 6}$	voltage drop during flyback					
	reverse	I_{defl} = 0.7 A	–	–2.0	–3.0	V
		I_{defl} = 1.0 A	–	–2.3	–3.5	V
	forward	I_{defl} = 0.7 A	–	+5.6	+6.1	V
		I_{defl} = 1.0 A	–	+5.9	+6.5	V
V_6	switching on threshold voltage		V_P – 1	–	V_P + 1.5	V
V_6	switching off threshold voltage		V_P – 1.5	–	V_P + 1	V
I_7	flyback current during flyback		–	–	±1	A
Guard circuit						
V_8	output voltage	guard on	7.5	8.5	10	V
V_8	output voltage	guard on; V_P = 8.2 V	6.9	–	V_P – 0.4	V
I_8	output current	guard on	5	–	–	mA
V_8	output voltage	guard off	–	–	0.4	V
I_8	output current	guard off; V_8 = 5 V	0.5	1	1.5	mA
$V_{8(ext.)}$	allowable external voltage on pin 8		0	–	13	V
		V_P ≤ 13 V	0	–	V_P + 0.3	V

Notes to the characteristics

1. Up to 60 V ≥ V_{FB} ≥ 40 V a decoupling capacitor C_{FB} = 22 µF (between pins 7 and 5) and a resistor R_{FB} = 100 Ω (between pin 7 and V_{FB}) are required (see Fig.4).
2. Saturation voltages of output stages A and B can be increased in the event of negative input currents $I_{1, 2}$ < –500 µA.
3. $D_i = \frac{I_{deflc}}{I_{idc}} \times \frac{I_{id}}{I_{defl}}$ with I_{deflc} = common mode deflection current and I_{idc} = common mode input current.
4. Deviation of the output slope at a constant input slope.
5. Frequency behaviour of G_{oi} and G_{ofb}:
   a) –3 dB open-loop bandwidth (–45°) at 15 kHz; second pole (–135°) at 1.3 MHz.
   b) open-loop gain at second pole (–135°) 55 dB.

TEST AND APPLICATION INFORMATION

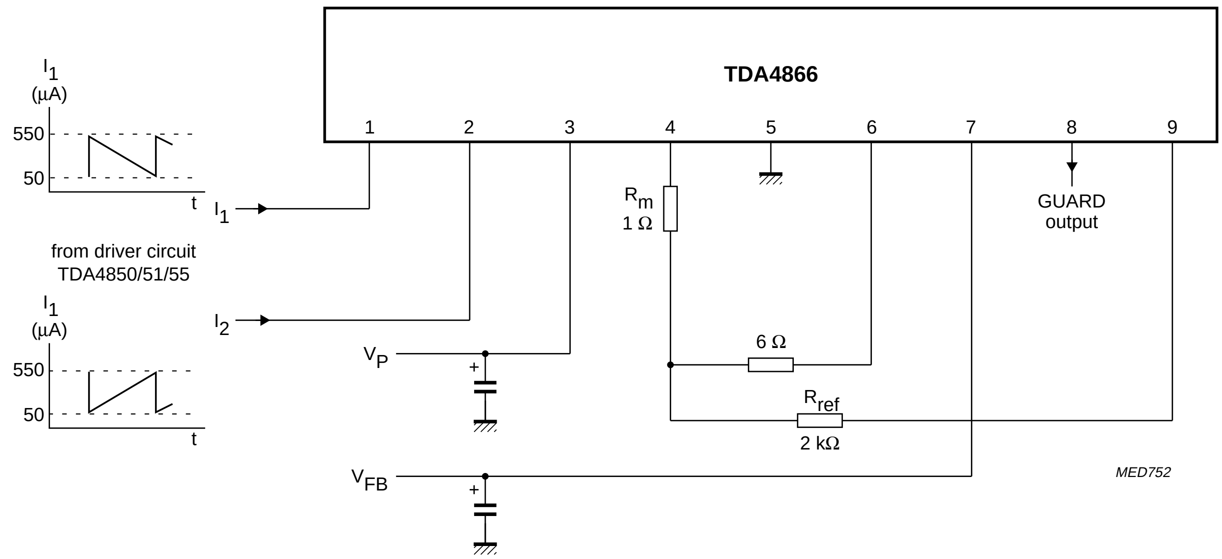
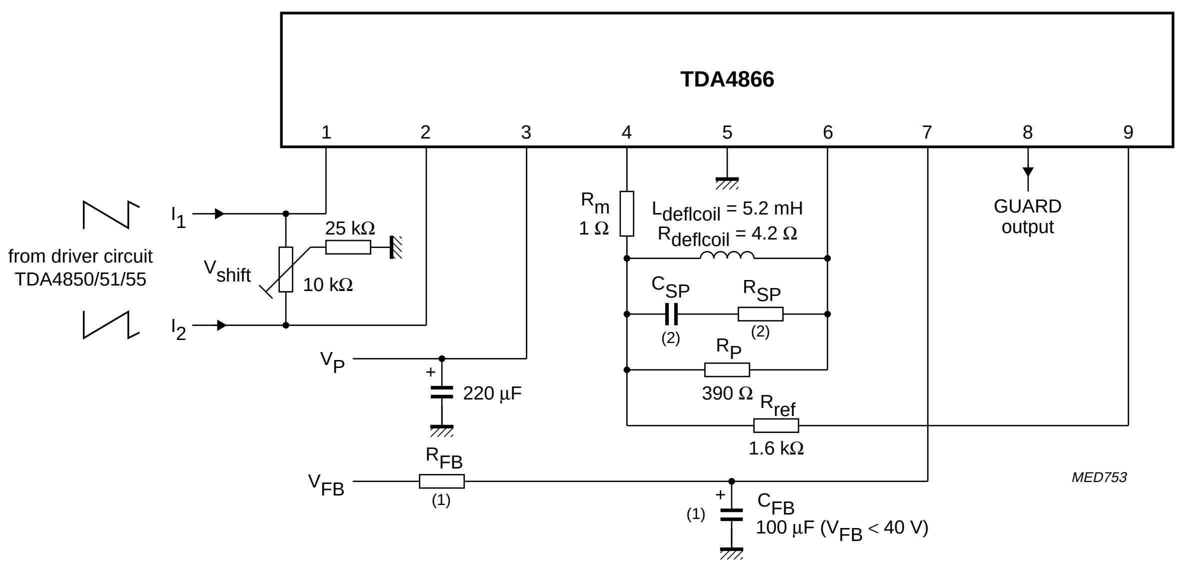


Fig.3 Test diagram.



(1) Up to 60 V ≥ V_{FB} ≥ 40 V R_{FB} = 100 Ω and C_{FB} = 22 µF are required.

(2) C_{SP} (20 nF to 220 nF) and R_{SP} = 10 Ω are strongly recommended. The value of C_{SP} depends on minimum t_{flb}/V_{FB}.

Fig.4 Application diagram with driver circuit TDA4850/51/55.

Example

SYMBOL	VALUE	UNIT
Values given from application		
$I_{defl(max)}$	0.71	A
$L_{deflcoil}$	5.2	mH
$R_{deflcoil}$	5.4 [= 4.2 + 7% + ΔR(ϑ)]	Ω
R_m	1 (+1%)	Ω
R_p	390	Ω
R_{ref}	1.6	kΩ
V_{FB}	35	V
T_{amb}	+50	°C
$T_{deflcoil}$	+75	°C
$R_{th\ j\text{-}mb}$	4	K/W
$R_{th\ mb\text{-}amb}$(1)	8	K/W
Calculated values		
V_P	8.6	V
t_{flb}	270	µs
P_{tot}	3.65	W
P_{defl}	0.9	W
P_{IC}	2.75	W
$R_{th\ tot}$	12	K/W
$T_{j(max)}$(2)	+83	°C

Notes

1. A layer of silicon grease between the mounting base and the heatsink optimizes thermal resistance.
2. $T_{j(max)} = P_{IC} \times (R_{th\ j\text{-}mb} + R_{th\ mb\text{-}amb}) + T_{amb}$

Calculation formula for supply voltage and power consumption

$V_{b1} = V_{6,3} + R_{deflcoil} \times I_{deflmax} - U'_L + R_m \times I_{defl(max)} + V_4$

$V_{b2} = V_6 + R_{deflcoil} \times I_{deflmax} + U'_L + R_m \times I_{defl(max)} + V_{4,3}$

for $V_{b1} > V_{b2}$: $V_P = V_{b1}$

for $V_{b2} > V_{b1}$: $V_P = V_{b2}$

with:

$U'_L = L_{deflcoil} \times 2I_{defl(max)} \times f_v$

f_v = vertical deflection frequency.

$$P_{tot} = V_P \times \frac{I_{defl(max)}}{2} + V_P \times 0.03\ A + 0.1\ W + V_{FB} \times I_{FB}$$

$$P_{defl} = \frac{1}{3}(R_{deflcoil} + R_m) \times I^2_{defl(max)}$$

$$P_{IC} = P_{tot} - P_{defl}$$

P_{IC} = power dissipation of the IC

P_{defl} = power dissipation of the deflection coil

P_{tot} = total power dissipation.

Calculation formula for flyback time (t_{flb})

$$t_{flb} = \frac{L_{deflcoil}}{R_{deflcoil} + R_m} \times \ln\left(\frac{1 + \frac{(R_{deflcoil} + R_m) \times I_{defl(max)}}{V_{FB} + V_{7r} - V_{6r}}}{1 - \frac{(R_{deflcoil} + R_m) \times I_{defl(max)}}{V_{FB} - (V_{7f} - V_{6f})}}\right) + t_{flboff}$$

with:

$t_{flb(off)}$ = flyback switch off time = 50 µs for this application ($t_{flb(off)}$ depends on V_{FB}, $I_{defl(max)}$, $L_{deflcoil}$ and C_{SP}).

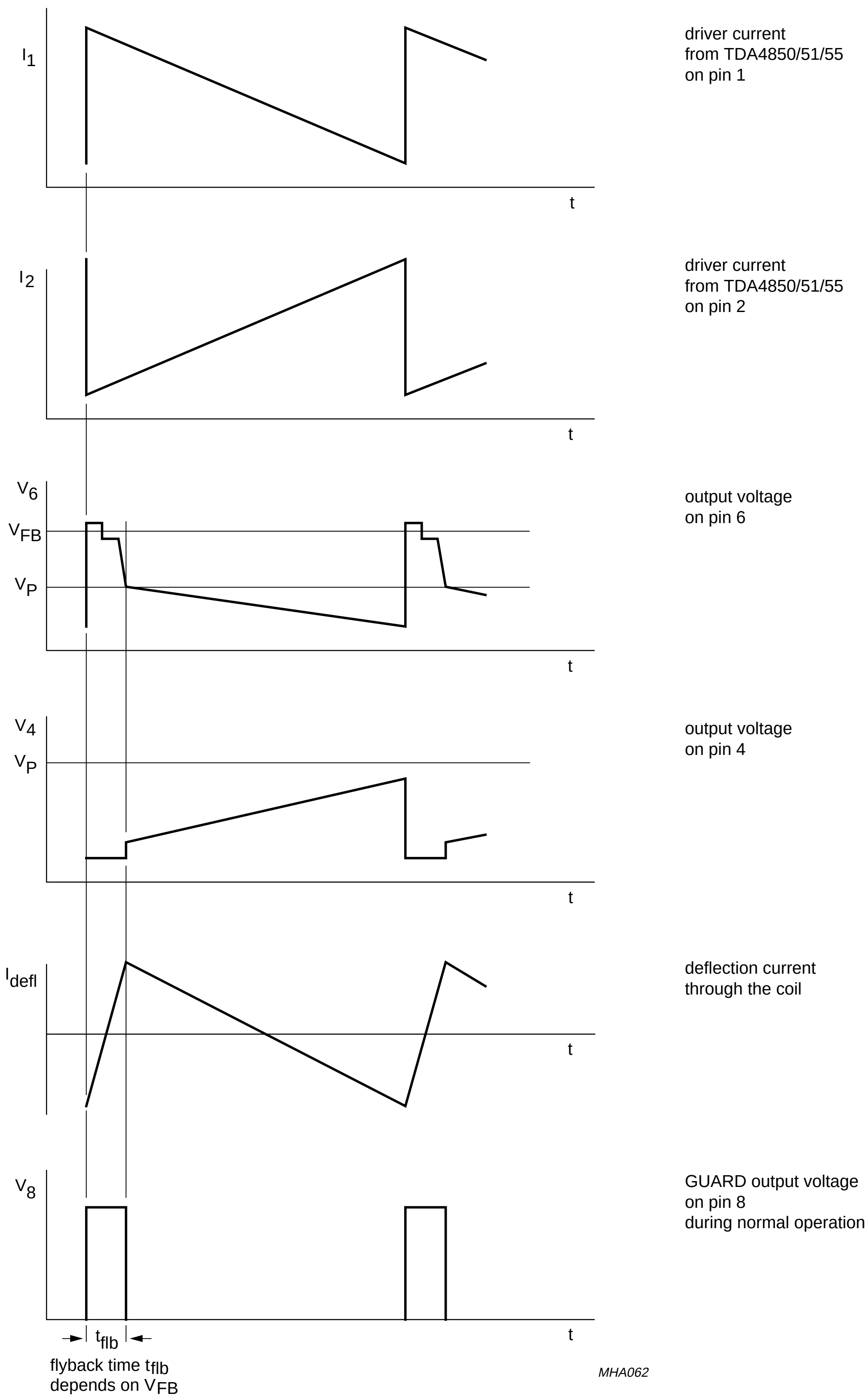


Fig.5 Timing diagram.

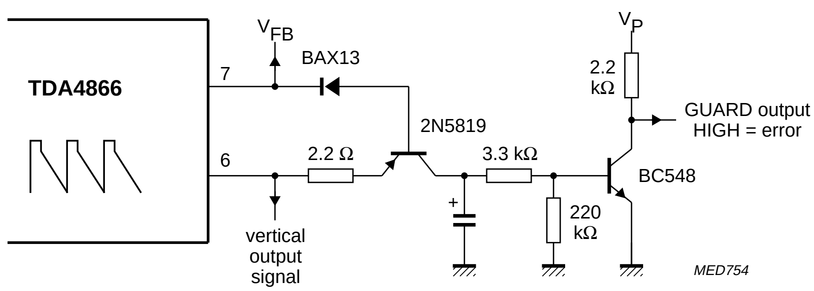


Fig.6 Application circuit for external guard signal generation.

INTERNAL PIN CONFIGURATION

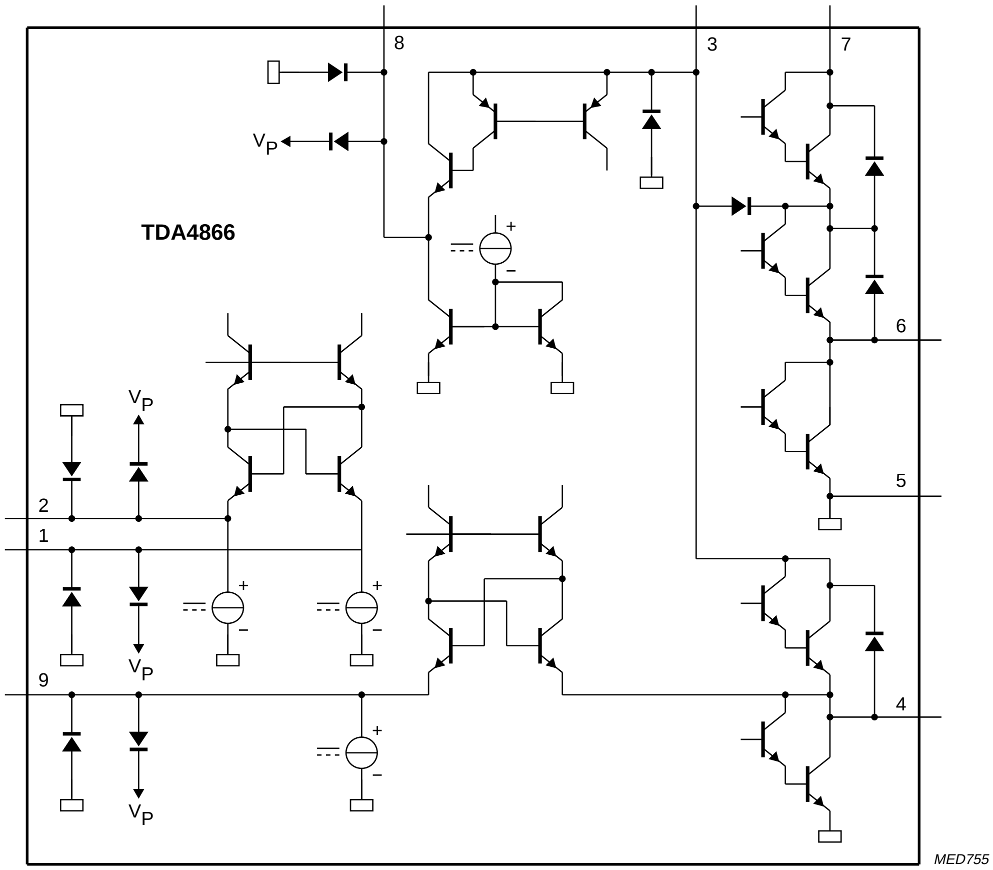
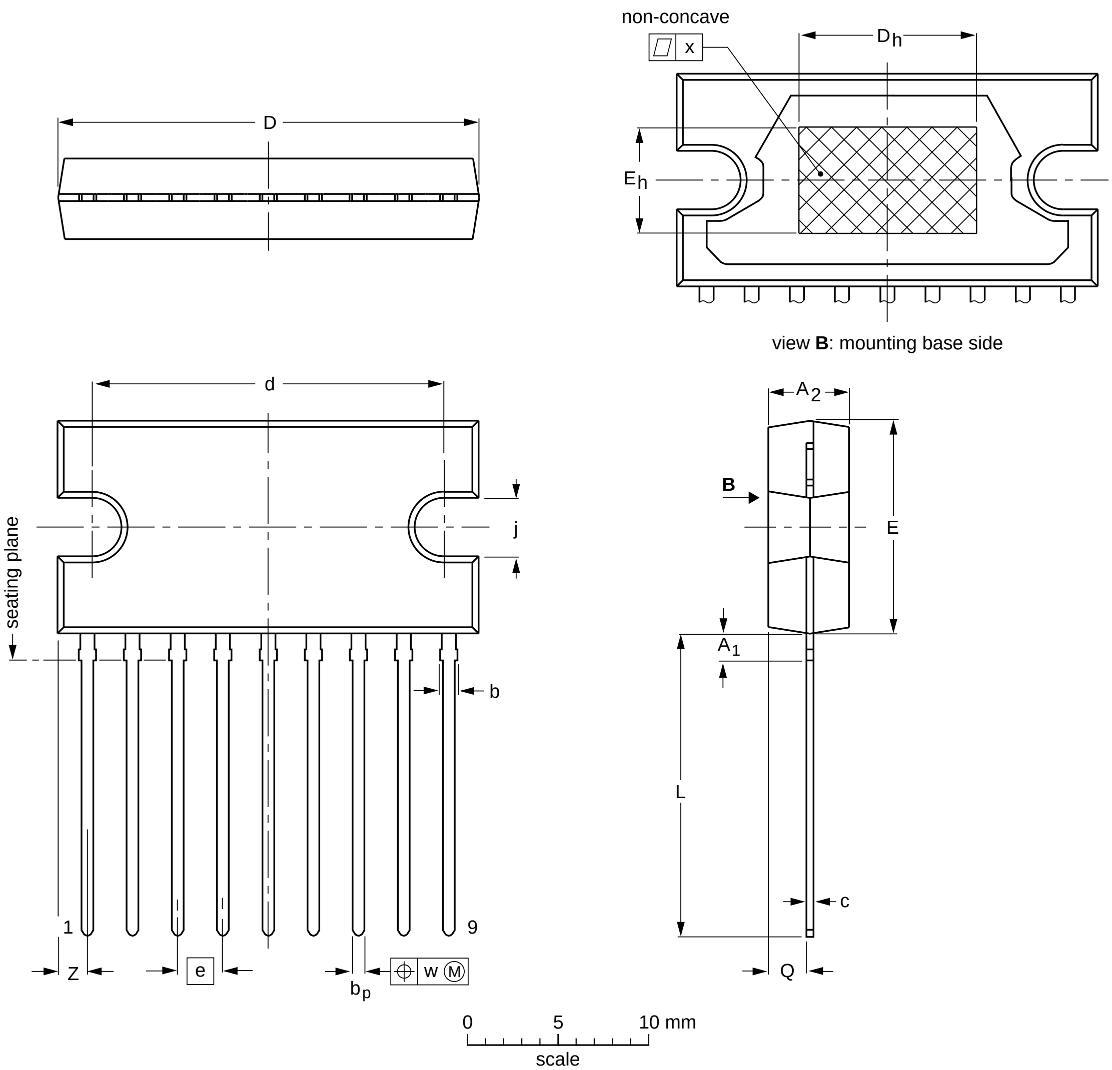


Fig.7 Internal circuits.

PACKAGE OUTLINE

SIL9P: plastic single in-line power package; 9 leads **SOT131-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A_1 max.	A_2	b max.	b_p	c	D(1)	d	D_h	E(1)	e	E_h	j	L	Q	w	x	Z(1)
mm	2.0	4.6 4.2	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						~~92-11-17~~ 95-03-11

SOLDERING

Plastic single in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

Philips Semiconductors – a worldwide company

Argentina: IEROD, Av. Juramento 1992 - 14.b, (1428) BUENOS AIRES, Tel. (541)786 7633, Fax. (541)786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. (02)805 4455, Fax. (02)805 4466

Austria: Triester Str. 64, A-1101 WIEN, P.O. Box 213, Tel. (01)60 101-1236, Fax. (01)60 101-1211

Belgium: Postbus 90050, 5600 PB EINDHOVEN, The Netherlands, Tel. (31)40 783 749, Fax. (31)40 788 399

Brazil: Rua do Rocio 220 - 5th floor, Suite 51, CEP: 04552-903-SÃO PAULO-SP, Brazil. P.O. Box 7383 (01064-970), Tel. (011)821-2333, Fax. (011)829-1849

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS: Tel. (800) 234-7381, Fax. (708) 296-8556

Chile: Av. Santa Maria 0760, SANTIAGO, Tel. (02)773 816, Fax. (02)777 6730

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. (852)2319 7888, Fax. (852)2319 7700

Colombia: IPRELENSO LTDA, Carrera 21 No. 56-17, 77621 BOGOTA, Tel. (571)249 7624/(571)217 4609, Fax. (571)217 4549

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. (032)88 2636, Fax. (031)57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. (358)0-615 800, Fax. (358)0-61580 920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex, Tel. (01)4099 6161, Fax. (01)4099 6427

Germany: P.O. Box 10 63 23, 20043 HAMBURG, Tel. (040)3296-0, Fax. (040)3296 213.

Greece: No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01)4894 339/4894 911, Fax. (01)4814 240

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd. Worli, Bombay 400 018 Tel. (022)4938 541, Fax. (022)4938 722

Indonesia: Philips House, Jalan H.R. Rasuna Said Kav. 3-4, P.O. Box 4252, JAKARTA 12950, Tel. (021)5201 122, Fax. (021)5205 189

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. (01)7640 000, Fax. (01)7640 200

Italy: PHILIPS SEMICONDUCTORS S.r.l., Piazza IV Novembre 3, 20124 MILANO, Tel. (0039)2 6752 2531, Fax. (0039)2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. (03)3740 5130, Fax. (03)3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. (02)709-1412, Fax. (02)709-1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. (03)750 5214, Fax. (03)757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TX 79905, Tel. 9-5(800)234-7381, Fax. (708)296-8556

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. (040)783749, Fax. (040)788399 (From 10-10-1995: Tel. (040)2783749, Fax. (040)2788399)

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. (09)849-4160, Fax. (09)849-7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. (022)74 8000, Fax. (022)74 8341

Pakistan: Philips Electrical Industries of Pakistan Ltd., Exchange Bldg. ST-2/A, Block 9, KDA Scheme 5, Clifton, KARACHI 75600, Tel. (021)587 4641-49, Fax. (021)577035/5874546

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc, 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. (02)810 0161, Fax. (02)817 3474

Portugal: PHILIPS PORTUGUESA, S.A., Rua dr. António Loureiro Borges 5, Arquiparque - Miraflores, Apartado 300, 2795 LINDA-A-VELHA, Tel. (01)4163160/4163333, Fax. (01)4163174/4163366

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